ELEC50010 Instruction Architecture & Compiler

**The Second Quarter Coursework**

**Group 6**

MIPS-compatible CPU datasheet

**General Description**

32-Bit MIPS CPU

Features

**Architecture**

**Instructions and State Machine**

The CPU are designed to execute following instructions:

|  |  |  |  |
| --- | --- | --- | --- |
| Code | Meaning | Code | Meaning |
| ADDIU | Add immediate unsigned (no overflow) | LWL | Load word left |
| ADDU | Add unsigned (no overflow) | LWR | Load word right |
| AND | Bitwise and | MTHI | Move to HI |
| ANDI | Bitwise and immediate | MTLO | Move to LO |
| BEQ | Branch on equal | MULT | Multiply |
| BGEZ | Branch on greater than or equal to zero | MULTU | Multiply unsigned |
| BGEZAL | Branch on non-negative (>=0) and link | OR | Bitwise or |
| BGTZ | Branch on greater than zero | ORI | Bitwise or immediate |
| BLEZ | Branch on less than or equal to zero | SB | Store byte |
| BLTZ | Branch on less than zero | SH | Store half-word |
| BLTZAL | Branch on less than zero and link | SLL | Shift left logical |
| BNE | Branch on not equal | SLLV | Shift left logical variable |
| DIV | Divide | SLT | Set on less than (signed) |
| DIVU | Divide unsigned | SLTI | Set on less than immediate (signed) |
| J | Jump | SLTIU | Set on less than immediate unsigned |
| JALR | Jump and link register | SLTU | Set on less than unsigned |
| JAL | Jump and link | SRA | Shift right arithmetic |
| JR | Jump register | SRAV | Shift right arithmetic |
| LB | Load byte | SRL | Shift right logical |
| LBU | Load byte unsigned | SRLV | Shift right logical variable |
| LH | Load half-word | SUBU | Subtract unsigned |
| LHU | Load half-word unsigned | SW | Store word |
| LUI | Load upper immediate | XOR | Bitwise exclusive or |
| LW | Load word | XORI | Bitwise exclusive or immediate |